UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,856,206 B1
APPLICATION NO. : 09/888663
DATED : February 15, 2005
INVENTOR(S) : Michael H. Perrott

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Please replace claims 1-39, beginning at Col. 21, line 46 through Col. 24, line 48 with the following claims:

1. A method of acquiring timing associated with an input data stream, comprising:
detecting whether transitions of the input data stream fall into a predetermined portion of a sample clock period of a sample clock utilized to sample the input data stream; and
evaluating whether a phase-locked loop (PLL) has acquired the timing of the input data stream according to occurrence of transitions of the input data stream in the predetermined portion of the sample clock period; and
wherein the evaluating further comprises determining over a plurality of time periods, each of the time periods including an increasing number of evaluation intervals, whether the PLL has acquired the timing of the input data stream according to a number of evaluation intervals having one or more transitions in the predetermined portion of the sample clock period.

2. A method of acquiring timing associated with an input data stream, comprising:
detecting whether transitions of the input data stream fall into a predetermined portion of a sample clock period of a sample clock utilized to sample the input data stream; and
evaluating whether a phase-locked loop (PLL) has locked to the timing of the input data stream according to occurrence of transitions of the input data stream in the predetermined portion of the sample clock period;
wherein the evaluating includes counting a number of evaluation intervals that have at least one transition in the predetermined portion of the clock period, generating a count indicative thereof and determining if lock is achieved according to the count; and
wherein the evaluation intervals are at least as long as a minimum period of frequency offset.

3. A method of acquiring timing associated with an input data stream, comprising:
detecting whether transitions of the input data stream fall into a predetermined portion of a sample clock period of a sample clock utilized to sample the input data stream;
evaluating whether a phase-locked loop (PLL) has locked to the timing of the input data stream according to occurrence of transitions of the input data stream in the predetermined portion of the sample clock period;
adjusting an output frequency of a variable frequency oscillator circuit in response to a determination that the PLL has not locked to the timing of the input data stream; and
wherein the output frequency is adjusted by changing a variable impedance associated with the oscillator circuit until lock is achieved.

4. The method as recited in claim 3, wherein the sample clock is a clock recovered from the input data stream.

5. The method as recited in claim 3, wherein the evaluating includes counting a number of evaluation intervals that have at least one transition in the predetermined portion of the clock period, generating a count indicative thereof and determining if lock is achieved according to the count.

6. The method as recited in claim 5, further comprising comparing the count to a threshold count to determine if lock is achieved.

7. The method as recited in claim 3 wherein the variable impedance is changed by adjusting at least a portion of the variable impedance in increasing increments around an initial impedance value.

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Claims (continued)

8. The method as recited in claim 7 further comprising sweeping another portion of the variable impedance linearly for each impedance setting resulting from adjusting at least a portion of the variable impedance in increasing increments around the initial impedance value.

9. The method as recited in claim 3, wherein the variable impedance is a capacitance.

10. The method as recited in claim 9 wherein the oscillator circuit is a tank circuit including an inductive element.

11. The method as recited in claim 3 wherein the oscillator circuit is a ring oscillator.

12. The method as recited in claim 3 wherein the oscillator circuit is a voltage controlled oscillator (VCO).

13. The method as recited in claim 3 wherein the predetermined portion of the clock period is adjacent to a clock edge used to sample the input data stream.

14. A method of acquiring a clock embedded in an input data stream, comprising varying an output of a variable oscillator until transitions of the input data stream occurring in a predefined phase zone of a sample clock sampling the input data stream occur below an acceptable rate, wherein the output of the variable oscillator is varied by varying an impedance of the variable oscillator.

15. A method of acquiring a clock embedded in an input data stream, comprising varying an output of a variable oscillator until transitions of the input data stream occurring in a predefined phase zone of a sample clock sampling the input data stream occur below an acceptable rate, wherein varying the output of the variable oscillator comprises varying at least one of a control voltage and a control current supplied to the variable oscillator.

16. An integrated circuit for receiving an input data stream and locking to a clock embedded in the input data stream using a phase-locked loop, the integrated circuit comprising:

a phase zone detect circuit coupled to determine if a transition of the input data stream occurs in a predetermined phase zone of a sample clock used to sample the input data stream;

a counter circuit coupled to the phase zone detect circuit to supply an indication of a number of evaluation intervals in which at least one bit error occurs;

a compare circuit coupled to compare the indication and a threshold value and to output a compare indication, thereby indicating if the phase-locked loop has locked to the input data stream;

a variable oscillator circuit forming part of the phase-locked loop;

a control circuit, responsive to the indication that lock is not achieved, to vary the output of the variable oscillator circuit; and

wherein the phase zone detect circuit includes a first data path and a second data path coupled to receive the input data stream, one of the first and second data paths being delayed with respect to the other, thereby defining the phase zone, and wherein an output signal supplied from the first and second data paths are coupled to a logic circuit to be logically compared.

17. The integrated circuit as recited in claim 16 wherein the first data path is a phase detector circuit coupled to provide an indication of phase error between a recovered clock being used to sample the input data stream and the input data stream.

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Claims (continued)

18. The integrated circuit as recited in claim 16 wherein the one of the first and second data paths is delayed by delaying one of the clock and the data of the input data stream supplied to the one of the first and second data paths.

19. The integrated circuit as recited in claim 16 wherein the second data path includes one or more selector circuits to select from a plurality of clock frequencies.

20. The integrated circuit as recited in claim 16 wherein the first and second data paths are logically compared in an exclusive OR circuit.

21. An integrated circuit for receiving an input data stream and locking to a clock embedded in the input data stream using a phase-locked loop, the integrated circuit comprising:

a phase zone detect circuit coupled to determine if a transition of the input data stream occurs in a predetermined phase zone of a sample clock used to sample the input data stream;

a counter circuit coupled to the phase zone detect circuit to supply an indication of a number of evaluation intervals in which at least one bit error occurs;

a compare circuit coupled to compare the indication and a threshold value and to output a compare indication, thereby indicating if the phase-locked loop has locked to the input data stream;

a variable oscillator circuit forming part of the phase-locked loop;

a control circuit, responsive to the indication that lock is not achieved, to vary the output of the variable oscillator circuit;

a variable impedance circuit forming part of the variable oscillator circuit; and

wherein the control circuit is responsive to the indication that lock is not achieved, to vary the variable impedance circuit to thereby adjust the output of the variable oscillator circuit.

22. The integrated circuit as recited in claim 21 wherein the control circuit adjusts the impedance by changing the impedance to successively above and then below an initial value to provide a gradually increasing swing around an initial impedance value.

23. The integrated circuit as recited in claim 21 wherein the phase-locked loop is determined to be locked to the input data stream if the indication from the count circuit indicates that the number of evaluation intervals in which at least one transition in a predetermined phase zone occurs is below a predetermined threshold value.

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Claims (continued)

24. The integrated circuit as recited in claim 21, wherein the variable impedance is a capacitance.

25. The integrated circuit as recited in claim 21 wherein the oscillator circuit is a tank circuit including an inductive element.

26. The integrated circuit as recited in claim 21 wherein the oscillator circuit is a ring oscillator.

27. The integrated circuit as recited in claim 21 wherein the oscillator circuit is a voltage controlled oscillator (VCO).

Signed and Sealed this

Eighth Day of August, 2006

JON W. DUDAS
Director of the United States Patent and Trademark Office